Amendments to Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Previously Presented) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. (Previously Presented) The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Previously Presented) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

4. (Original) The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. - 6. (Canceled)

7. (Previously Presented) The method of claim 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. (Original) The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. (Previously Presented) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. (Original) The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Previously Presented) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said trench and said series of trenches.

12. (Original) The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. - 14. (Canceled)

15. (Previously Presented) The method of claim 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

17. (Previously Presented) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. (Original) The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. (Original) The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. (Original) The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. (Previously Presented) The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. (Previously Presented) The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

23. (Previously Presented) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Previously Presented) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Previously Presented) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions.

26. (New) The method of claim 1, wherein said polishing comprising applying a liquid consisting essentially of deionized water at a substantially neutral pH.

27. (New) The method of claim 9, wherein said polishing comprising applying a liquid consisting essentially of deionized water at a substantially neutral pH.